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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,234	09/03/2003	Bin Yu	H1491	4829

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,234	YU ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/15/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *7-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0903*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 09/03/2003 through 03/15/2005, claims 1-18 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 09/03/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I: Claims 1-6 and 15-18, drawn to a semiconductor device, classified in class 257, subclass 384.

Group II: Claims 7-14, drawn to process of making a semiconductor device, classified in class 438, and subclass 151.

4. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of following can be shown: (1) that the process as claimed can be use to make other and materially different product or by hand, or (2) that the product as claimed can be made by another and materially different process. (MPEP § 806.05(f)). In the instant case, unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by other and materially different processes from those of the group II invention.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, the fields of search are not co-extensive. Therefore, separate examination would be required and restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Attorney Brian E. Ledell on 03/15/2005, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-6 and 15-18. Affirmation of this election of claims must be made by applicant in replying to this Office action.

Claims 7-14 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

Specification

8. The specification is objected to for the following reason: On page 3, paragraph [0011], figure No. "2B" should be corrected to –1B--.

9. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claim(s) 1-6 and 15-18 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,395,589 to Yu.

Regarding claim 1, Yu discloses a semiconductor device, as shown in figs. 7-17, comprising:

an insulator 202,

a semiconductor layer formed on the insulator 202, the semiconductor layer including a fin portion (under gate structure 246) corresponding to a channel of the semiconductor device;

a source region 222 formed at a first end of the semiconductor layer, a height of the source region 222 being higher than that of the fin;

a drain region 224 formed at a second end of the semiconductor layer, a height of the drain region 224 being higher than that of the fin; and

a metal gate region 246 formed over to overlap at a top surface and at least one side surface of the fin.

Regarding claim 15, Yu discloses a FinFET device, as shown in figs. 7-17, comprising:

an insulator 202;

a semiconductor layer formed on the insulator, the semiconductor layer

including a fin portion (under gate structure 246) corresponding to a channel of the semiconductor device;

a source region 222 formed from a first end of the semiconductor layer, a height of the source region 222 being higher than that of the fin and a width of the source region 222 being wider than that of the fin;

a drain region 224 formed from a second end of the semiconductor layer, a height of the drain region being higher than that of the fin and a width of the drain region being wider than that of the fin;

a metal gate region 246 formed to overlap at a top surface and at least one side surface of the fin; and

sidewalls spacers 242 formed adjacent at least portions of the metal gate region 246.

Regarding claims 2-6 and 16-18, Yu disclose the device comprising all claimed limitations. See figs. 7-17 and co. 4, line 43 to col. 7, line 67.

12. Claim(s) 1-2, 4-6, and 18 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent Application No. 2004/0227187 to Cheng et al.

Regarding claim 1, Cheng discloses a semiconductor device, as shown in figs. 8-9, comprising:

an insulator 102;

a semiconductor layer formed on the insulator 102, the semiconductor

layer including a fin portion 104 corresponding to a channel of the semiconductor device;

a source region 106 formed at a first end of the semiconductor layer, a height of the source region 106 being higher than that of the fin 104;

a drain region 108 formed at a second end of the semiconductor layer, a height of the drain region 108 being higher than that of the fin 104 (figs. 8); and

a metal gate region 94 formed over to overlap at a top surface and at least one side surface of the fin 84 (figs. 8(E, F) and page 4, paragraph [0043]).

Regarding claim 2, Cheng discloses the device wherein the metal gate region 94 overlaps the top surface and two side surfaces of the fin 84. See figs. 8.

Regarding claim 4, Cheng discloses the device wherein the source and drain regions are silicided. See paragraphs [0036]-[0043].

Regarding claim 5, Cheng discloses the device wherein a distance between the insulator and the metal gate region is about 500 Å to about 700 Å and a distance between the insulator and a top of the source or the drain region is about 600 Å to about 1000 Å. See page 4, paragraph [0042]; and page 6, claim 24.

Regarding claim 6, Cheng discloses the device wherein the metal gate comprises at least one of tungsten, titanium, nickel, TaSiN, and TaN. See page 5, claim 9.

Regarding claim 18, Cheng/Shih discloses the FinFET wherein a thickness of the fin portion ranges from about 500 h to about 700 A and a thickness of the source and drain regions ranges from about 600 Å to about 1000 Å. See page 4, paragraph [0042]; and page 6, claim 24 of Cheng.

Claim Rejections - 35 U.S.C. § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim(s) 3, and 15-17 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent Application No. 2004/0227187 to Cheng et al., in view of Wu, U.S. Patent No. 6,455,383, and further in view of the following remarks.

Regarding claim 3, Cheng discloses the device comprising all claimed limitations, except for oxide sidewalls formed adjacent the metal gate region in an area adjacent the top surface of the fin.

Wu discloses a semiconductor device, as shown in figs. 1-2, comprising a semiconductor including a fin portion (under the gate structure 102a) corresponding to a channel of the semiconductor device; a source and a drain regions 105a/107a/108a formed from a first and a second ends of the semiconductor, wherein a height of the source region and a height of the drain region being higher than that of the fin (the source/drain regions raised above the substrate 100 whereas the fin/channel region positioned within the substrate) and a width of the source region and a width of the drain region being wider than that of the fin; a metal gate region 102a formed to overlap at a top surface and at least one side surface of the fin; and

Sidewalls spacers 106a formed adjacent portions of the metal gate region 102a.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Cheng so that it would further include sidewall spacers as those of Wu in order to provide protection to the gate from external effects and from short circuit to the source/drain contacts.

Regarding claim 15, Cheng discloses a FinFET device, as shown in figs. 8-9, comprising:

an insulator 102;

a semiconductor layer formed on the insulator 102, the semiconductor layer including a fin portion 104 corresponding to a channel of the semiconductor device;

a source region 106 formed from a first end of the semiconductor layer, a height of the source region 106 being higher than that of the fin 104 and a width of the source region 106 being wider than that of the fin 104;

a drain region 108 formed from a second end of the semiconductor layer, a height of the drain region 108 being higher than that of the fin 104 and a width of the drain region 108 being wider than that of the fin 104 (see figs. 8-9);

a metal gate region 94 formed to overlap at a top surface and at least one side surface of the fin 84 (figs. 8).

Cheng is silent about sidewalls spacers formed adjacent at least portions of the metal gate region.

Wu discloses a semiconductor device, as shown in figs. 1-2, comprising a semiconductor including a fin portion (under the gate structure 102a) corresponding to a channel of the semiconductor device; a source and a drain regions 105a/107a/108a formed from a first and a second ends of the semiconductor, wherein a height of the source region and a height of the drain region being higher than that of the fin (the source/drain regions raised above the substrate 100 whereas the fin/channel region positioned within the substrate) and a width of the source region and a width of the drain region being wider than that of the fin; a metal gate region 102a formed to overlap at a top surface and at least one side surface of the fin; and

Sidewalls spacers 106a formed adjacent portions of the metal gate region 102a.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Cheng so that it would further include sidewall spacers as those of Wu in order to provide protection to the gate from external effects and from short circuit to the source/drain contacts.

Regarding claim 16, Cheng/Shih disclose the FinFET device comprising all claimed limitation, except for explicitly teach that the sidewall spacers having a width ranging from about 150 Å to about 1000 Å. However, Cheng/Shih teach that the width of spacers determines the profile of the source/drain regions implantation (see col. 4, lines 58-60 of Shih).

Hence, It would have been obvious to one having ordinary skill in the art at the time the invention was made that the width of the spacers can be varied or modified in a large range, which could include from about 150 Å to about 1000 Å, depending on the desired profile of the source/drain region implantation.

Regarding claim 17, Cheng/Shih disclose the FinFET wherein the source and drain regions are silicided. See paragraphs [0036]-[0047] of Cheng.

Conclusion

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
March 31, 2005